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[STRUCTURE, FABRICATION METHOD AND OPERATION METHOD OF FLASH MEMORY]

Abstract of Disclosure

A structure of a flash memory, having a deep P-well formed in an N-type substrate, an N-well formed in the deep P-well, a stacked gate structure formed on the substrate, an N-type source region and an N-type drain region formed in an N-well at two respective sides of the stacked gate, where the N-type source region is in electric contact with the N-well, a P-well formed in the N-well to encompass the N-type source region and to extend towards the N-type drain region through the portion under the stacked gate, and a contact window formed at the junction of the N-type source region and the P-well to electrically short circuit the N-type source region and the P-well. The flash memory uses F-N tunneling effect for programming and the channel F-N tunneling effect to perform the erase operation.

Figures